Articles

Establishing Efficient Electrical Contact to the Weak Crystals of Triethylsilylethynyl Anthradithiophene

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Triethylsilylethynyl anthradithiophene (TES ADT) forms weak van der Waals crystals in the solid state because its bulky TES side groups limit intermolecular interactions. Consequently, TES ADT melts easily and locally when it experiences heat conduction from the metal evaporation process to form electrical contacts. The performance of TES ADT thin-film transistors is thus highly dependent upon the manner in which electrical contacts are established to the organic semiconductor. Bottom-contact TES ADT thin-film transistors in which the electrodes are fabricated prior to the organic semiconductor deposition routinely exhibit a charge-carrier mobility of 0.11 ± 0.05 cm^2/V·s. Top-contact thin-film transistors with electrodes patterned directly on top of TES ADT by metal evaporation through a shadow mask, on the other hand, exhibit highly variable device characteristics with a charge-carrier mobility 0.03 ± 0.03 cm^2/V·s. To avoid thermal damage to TES ADT during electrode fabrication, we separately defined gold source and drain electrodes on elastomeric stamps and then laminated the electrodes against TES ADT to form top-contact devices. These laminated top-contact thin-film transistors exhibit device characteristics with minimal current−voltage hysteresis and an enhanced charge-carrier mobility of 0.19 ± 0.06 cm^2/V·s.

Introduction

Solution-processable organic semiconductors[1−6] are desirable because they enable low-cost deposition methods, such as spin casting or drop casting, for fabricating organic thin-film transistors. Additionally, the morphology of solution-processable organic semiconductors can be manipulated by controlling the solvent evaporation rate during deposition,[1,3] or with straightforward postdeposition solvent−vapor annealing[7] and thermal annealing.[8] In particular, we have studied triethylsilylethynyl anthradithiophene (TES ADT),[4,7,9] a p-type organic semiconductor that has previously been shown to exhibit a charge-carrier mobility ≥0.1 cm^2/V·s in bottom-contact thin-film transistors.[7,9] The bulky TES side groups make this material readily soluble[9] and facilitate low-cost solution deposition techniques, but they limit the intermolecular interactions in the solid state. Examination of the compound's crystal packing (see schematic of crystal packing in Figure 1) reveals minimal π-face interactions between adjacent molecules. The π-orbital overlap that does exist in TES ADT, however, provides sufficient atomic contact to allow efficient charge transport.[10] The material thus melts at a relatively low temperature (≤160 °C) with a small melting enthalpy (∼26 J/g) compared to pentacene, which melts >200 °C[11] with a sublimation enthalpy of ∼564 J/g[12] or tetracene, which melts at 340 °C with a melting enthalpy of 695.6 J/g.[13] Consequently, TES ADT requires

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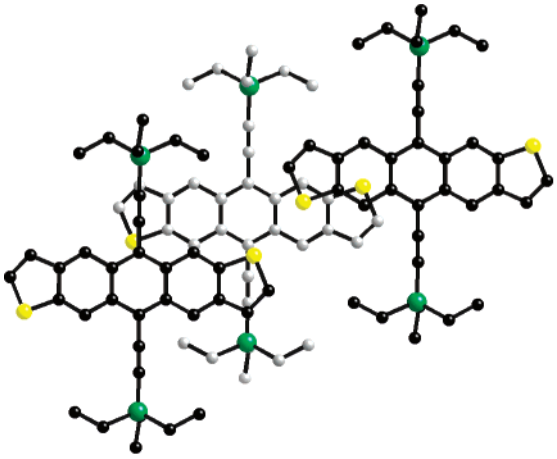

Figure 1. View of the TES ADT crystal packing normal to the aromatic π-faces showing minimal π-overlap between adjacent molecules. Yellow represents sulfur, green represents silicon, and black and gray represent carbon atoms on different planes. We note that the placement of the sulfur atoms within a TES ADT crystal is disordered; i.e., it is equally probable to find the mirror image of the molecules in the figure where the sulfur atoms are flipped.

significantly less energy to disorder its crystals compared to pentacene or tetracene. This physical characteristic of TES ADT has allowed us to routinely spin-cast amorphous thin films whereas other solution-processed organic semiconductors tend to crystallize as the solvent rapidly evaporates during the spin-casting process.[1] TES ADT can then be controllably crystallized in a subsequent solvent−vapor annealing step.[7] The ease with which the material melts has also enabled us to pattern TES ADT using selective UV illumination or with PDMS stamps.[14] Limiting TES ADT to the channel region using these patterning schemes has effectively reduced parasitic leakage and off currents in these thin-film transistors. On the down side, TES ADT has a tendency to melt easily and locally when it is directly exposed to gold evaporation during the electrode fabrication process of top-contact thin-film transistors. As such, the device performance of these top-contact TES ADT thin-film transistors[15,16] is poor. In fact, many of the devices fabricated in this fashion do not exhibit any field effect characteristics. Of the 26 devices that are functional, the average charge-carrier mobility is 0.04 ± 0.03 cm^2/V·s; this value is statistically lower than the charge-carrier mobility we had previously reported for bottom-contact TES ADT thin-film transistors (0.11 ± 0.05 cm^2/V·s). When we avoid exposing the organic semiconductor to the electrode fabrication process and form top-contact devices by bringing predefined source and drain electrodes into contact and laminating them against TES ADT,[17−20] these devices routinely exhibit an enhanced charge-carrier mobility of 0.19 ± 0.06 cm^2/V·s. Our results reveal the extent that chemical derivatization of organic semiconductors can influence their physical properties and emphasize the need to use patterning strategies that specifically account for their materials properties when establishing electrical contact during device fabrication.

Experimental Section

TES ADT Thin-Film Transistor Fabrication. TES ADT was synthesized according to previously published procedures.[4] Bottom- and top-contact TES ADT thin-film transistors were fabricated on prime-grade, heavily doped silicon wafers with 100 nm of thermally grown silicon dioxide (Nova Electronics), which served as the common gate and gate dielectric, respectively. In bottom-contact thin-film transistors, the source and drain electrodes, consisting of a 5 nm titanium strike layer and 40 nm gold, were patterned directly on the silicon dioxide surface through a shadow mask by electron-beam evaporation. The channel lengths were 100 μm and the channel widths were 1000 μm. Following electrode deposition, the patterned silicon platform was sonicated in deionized water for 3 min, dried under a stream of nitrogen, and placed in a UV/ozone chamber for 10 min. A 2 wt % solution of TES ADT in toluene (Fisher Scientific) was then spin-coated on the UV/ozone-treated transistor platform at 1000 rpm. Following deposition (the TES ADT film is amorphous), the as-spun thin-film transistors were heated in air at 90 °C for 2 min to remove residual solvent and then annealed in a dichloroethane-vapor-rich environment for 2−10 min at room temperature to crystallize as-spun TES ADT.[7] To eliminate parasitic leakage currents, individual thin-film transistors were isolated by scratching through the TES ADT thin film with a razor blade in the nonchannel regions of the devices. Isolation of devices can also be accomplished over large areas by selective UV illumination during crystallization or with PDMS stamps postcrystallization.[14]

To fabricate top-contact transistors, TES ADT solution was spin-coated on highly doped silicon wafers with 100 nm of thermally grown silicon dioxide immediately following the cleaning procedures outlined above, and TES ADT spun films were crystallized by exposure to solvent vapors.[7] Gold source and drain electrodes (40 nm) were defined directly on the crystalline TES ADT thin films by gold evaporation through a shadow mask at either 1 or 10 Å/s. Individual transistors were isolated by scratching through the TES ADT thin film in the nonchannel regions. The electrodes for the laminated top-contact thin-film transistors[17−20] were fabricated separately on a poly(dimethylsiloxane), PDMS, stamp with raised features resembling the source and drain electrodes. The PDMS stamps were created by casting and curing Sylgard 184 PDMS prepolymer (Dow Corning) against a silicon master previously patterned by conventional photolithography.[21] The PDMS surface was then activated by exposure to UV/ozone for 8 min. Immediately following UV/ozone treatment, 2 nm of titanium and 15−18 nm of gold were sequentially deposited on the raised and recessed regions of the PDMS stamps—but not on the sidewalls—resulting in electrically isolated gold electrodes.[22] The titanium layer permanently adheres the gold layer to the UV/ozone-activated PDMS stamps.[17] To fabricate laminated top-contact thin-film transistors, isolated gold contact pads, consisting of a 2 nm titanium strike layer and 40 nm of gold, were also defined on the silicon

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dioxide surface around the exterior of the crystalline TES ADT thin film. The PDMS stamp with gold source and drain features was then nondestructively laminated against the crystalline TES ADT thin film, ensuring that the electrodes contacted both the crystalline TES ADT thin film and the gold contact pads to complete the laminated top-contact thin-film transistors. We probed the current−voltage characteristics by making direct contact to the gold contact pads.

Sample Characterization. Electrical characterization of all the TES ADT thin-film transistors was performed using a Karl Suss Probe Station and an Agilent 4156C Parameter Analyzer. Charge-carrier mobilities were extracted from the current−voltage characteristics by plotting the square root of the source−drain current versus gate voltage at a source−drain voltage of −20 V. Atomic force microscopy (AFM) images were collected in tapping mode with a Veeco Instruments Dimension 3100 Multimode AFM using a standard tapping tip (Nano Devices Metrology Probes TAP150). Scanning surface potential measurements (SSPM)[23−25] were collected with a Veeco Instruments Bioscope atomic force microscope interfaced with a Nanoscope IV controller and operated in SSPM mode to directly measure the local surface potential of TES ADT thin-film transistors in operation. The data were collected in two passes with a conductive tapping tip (MikroMasch NSC15/Ti−Pt). On the first pass, the microscope was operated in tapping mode to acquire the surface topography of the transistor channel with the source, drain, and gate electrodes grounded. On retracing of the same topography scan, the tip was raised 10 nm off the surface and an ac electric field was applied at the resonance frequency of the tip. During the second scan, a feedback loop was used to measure and null the phase shift between the tip and surface by adding a dc bias to the tip.[23] This dc bias was applied to nullify the phase shift that corresponds to the local electrostatic surface potential, or the contact potential difference (CPD) between the tip and the surface. Surface potential profiles were measured on actively biased bottom- and top-contact transistors operating in the linear regime. An external power source supplied the source−drain and gate voltages to power the device. A bias of −2 V was applied to the drain while the gate bias was stepped from 0 to −20 V in −4 V increments. Differences in work function between the tip and surface are removed by subtracting the scans collected at zero drain and gate biases from the scans collected at nonzero biases.[24] All scans were conducted in a nitrogen-purged environment. Since the scan window of the AFM is limited to 100 μm, each contact region was scanned sequentially to span the entire channel region.

X-ray photoelectron spectroscopy (XPS) analysis was performed with a Physical Electronics ESCA 5700 spectrophotometer equipped with a monochromatic Al Kα X-ray source, a hemispherical electron analyzer, and a low-energy electron flood gun for charge compensation of insulating samples. Samples were introduced through a preparation chamber before being transferred into the analysis chamber at 2×10^{-10} Torr. The samples were typically analyzed at a takeoff angle of 45°, defined as the angle between the sample and the detector. Samples containing a 2 nm gold overlayer were analyzed at a larger takeoff angle of 80° to probe the underlying TES ADT. All spectra were collected at a pass energy of 11 eV.

X-ray diffraction experiments were conducted with a Scintag X1 $\theta-\theta$ diffractometer equipped with a Cu Kα X-ray source and a solid-state detector. Samples were analyzed from $2\theta = 0$ to $2\theta = 60°$ with a resolution of 0.04° and a dwell time of 5 s.

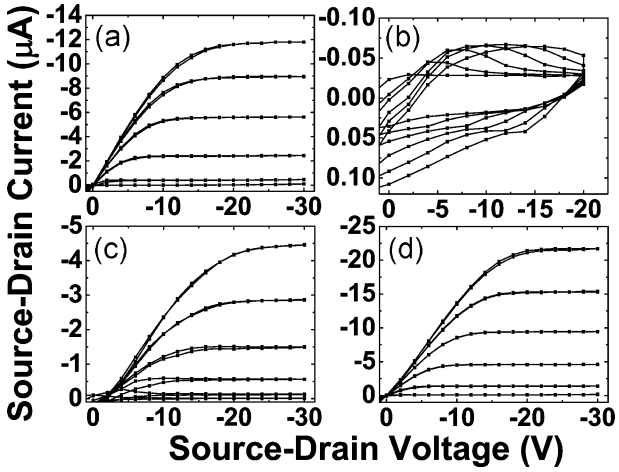

Figure 2. Current−voltage characteristics of (a) a bottom-contact TES ADT thin-film transistor, (b) a top-contact TES ADT thin-film transistor with electrodes defined by direct evaporation at 1 Å/s, (c) a top-contact TES ADT thin-film transistor with electrodes defined by direct evaporation at 10 Å/s, and (d) a top-contact TES ADT thin-film transistor with laminated electrodes. The current−voltage characteristics were collected between gate voltages of 0 and −20 V, in increments of −4 V.

Results and Discussion

Figure 2 shows the current−voltage characteristics of representative bottom- and top-contact TES ADT thin-film transistors with channel lengths of 100 μm and channel widths of 1000 μm. The bottom-contact TES ADT thin-film transistor exhibited high currents (Figure 2a) and an extracted charge-carrier mobility of 0.2 cm^2/V·s. Of 121 devices tested, the average charge-carrier mobility was 0.11 ± 0.05 cm^2/V·s. In stark contrast, the top-contact TES ADT thin-film transistor having the same channel geometry and dimensions as gold source and drain electrodes evaporated at 1 Å/s (Figure 2b) did not exhibit any field effect. Of approximately 50 devices fabricated, only 25% of the devices was functional, with the functional devices exhibiting an average charge-carrier mobility of 0.03 ± 0.02 cm^2/V·s. Current−voltage characteristics of a top-contact thin-film transistor with gold source and drain electrodes evaporated at 10 Å/s (also the same channel geometry and dimensions) are shown in Figure 2c. Although the performance of this device was slightly better (0.08 cm^2/V·s) than that of the top-contact device with gold electrodes deposited at 1 Å/s, its performance did not exceed that of the bottom-contact device. We fabricated approximately 35 top-contact TES ADT thin-film transistors with electrodes deposited at 10 Å/s, approximately half of those devices showed field-effect characteristics; the average charge-carrier mobility of functional devices was 0.07 ± 0.03 cm^2/V·s.

These results are surprising considering that top-contact pentacene[26−29] and polythiophene[30] thin-film transistors

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routinely outperform bottom-contact devices having equivalent channel geometry and dimensions. The difference in performance between these top- and bottom-contact thin-film transistors has been attributed to the presence of structural defects at the electrode−channel interface in thin-film transistors.[31,32] Specifically, in bottom-contact thin-film transistors, the organic semiconductor is deposited on both the predefined electrodes and the dielectric surface. Differences in topography can thus lead to discontinuities and defects in the organic semiconductor thin film at the electrode−channel interfaces.[31,32] Since charge injection and charge extraction occur at these interfaces, the presence of defects can severely limit the performance of the resulting bottom-contact thin-film transistor.[24,27] In contrast, the organic semiconductor is deposited on a topographically flat dielectric surface in top-contact thin-film transistors before the source and drain electrodes are patterned on top of the organic semiconductor thin film. This process thus eliminates the presence of defects at the electrode−channel interface.[30,32,33]

Contrary to this documented precedence, the performance of our top-contact TES ADT thin-film transistors is consistently inferior compared to that of the bottom-contact TES ADT devices of comparable geometry and channel dimensions. That the performance of top-contact devices is inferior compared to that of bottom-contact devices has recently been observed in tetracene single-crystal thin-film transistors.[34] While de Boer et al. attributed the "damage" to the direct evaporation of gold onto tetracene single crystals, physical explanations for this "damage" were not provided. To probe the origin of this anomaly in our TES ADT thin-film transistors, we carried out X-ray photoelectron spectroscopy (XPS) experiments on crystalline TES ADT to determine if direct gold evaporation causes any chemical degradation or photo-oxidation. Specifically, XPS was carried out on crystallized TES ADT and then on the same film after it had been subjected to gold evaporation. To detect TES ADT through the evaporated gold, only 2 nm of gold were deposited on crystalline TES ADT. We collected high-resolution elemental XPS scans in the carbon, sulfur, silicon, and oxygen regions; these spectra are shown in Figure 3. The intensities of the scans acquired after gold evaporation are attenuated because the presence of the gold overlayer increases the photoelectron path length. Aside from the intensity attenuation, however, the spectra collected on TES ADT before and after gold evaporation appear nearly identical. Specifically, the shapes and positions of the carbon, sulfur, and silicon peaks remain unchanged, and the spectra collected in the vicinity of 530 eV reveal no detectable oxygen. That the XPS spectra remain unchanged is a good

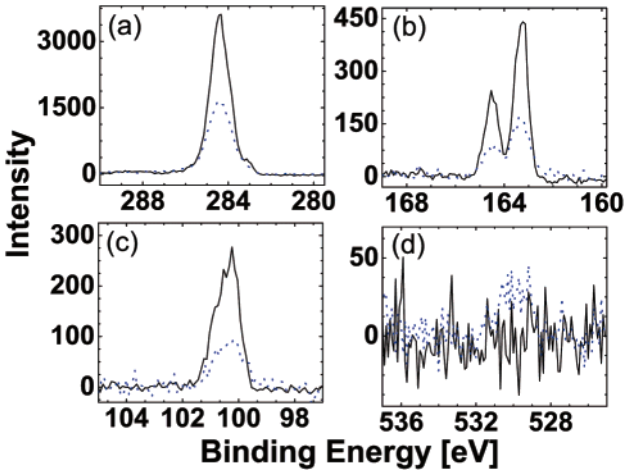

Figure 3. High-resolution X-ray photoelectron spectroscopy elemental scans of (a) carbon, (b) sulfur, (c) silicon, and (d) oxygen from a crystalline TES ADT film on a silicon substrate before (solid line) and after (dashed line) gold evaporation at 1 Å/s. There is no indication of chemical change after the gold evaporation.

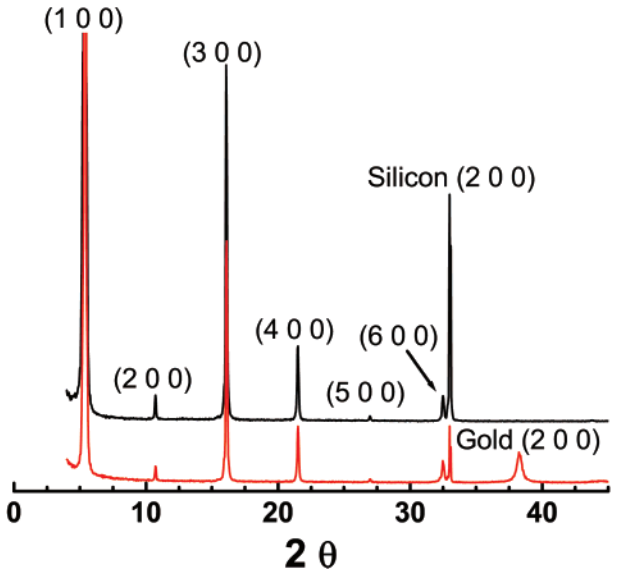

Figure 4. X-ray diffraction spectra of a crystalline TES ADT film obtained on a silicon substrate before (upper line) and after (bottom line) gold evaporation at 1 Å/s. There are no detectable changes in the peak shapes or positions after exposure to gold evaporation.

indication that TES ADT did not experience any chemical changes during gold evaporation.

In addition to probing the chemical environment of TES ADT, we examined its crystal structure before and after gold evaporation by X-ray diffraction (XRD). We collected XRD spectra on crystalline TES ADT before and after (Figure 4, top and bottom line, respectively) 40 nm of gold had been deposited at 1 Å/s. The annealed TES ADT thin film before gold evaporation (Figure 4, top line) is crystalline; we observe diffraction peaks associated with the (100), (200), (300), etc. planes of the lattice. We also observe a peak at $2\theta \sim 33°$ that corresponds to the (200) plane of the underlying single-crystal silicon substrate.[35] The XRD spectrum obtained from the film below the gold overlayer reveals the same Bragg diffraction peaks (Figure 4, bottom line). We do not detect any shifts in the peak positions or any line

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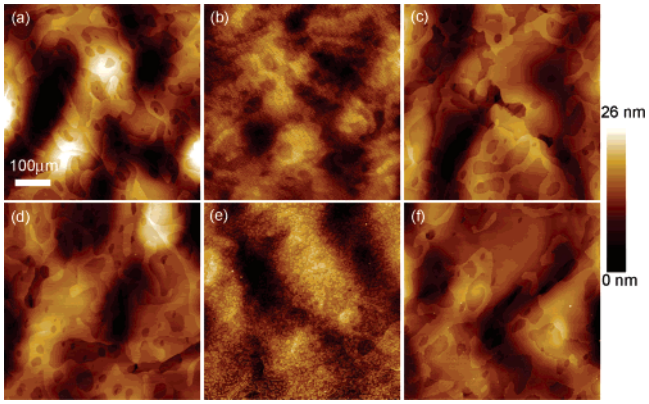

Figure 5. Atomic force microscopy images of crystalline TES ADT (a) before gold evaporation, (b) after removal of the gold overlayer that was originally evaporated at 1 Å/s, and (c) in the regions protected by a shadow mask. The images shown in (d)−(g) are analogous to those shown in (a)−(c), except that TES ADT was subjected to gold evaporation at 10 Å/s.

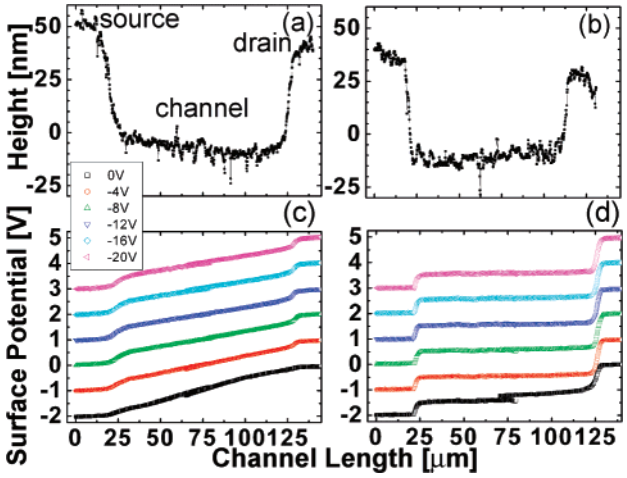

Figure 6. Topography of the channel regions of a bottom- (a) and a top-contact TES ADT thin-film transistor in which the electrodes were deposited at 10 Å/s (b) and the surface potential measurements of the respective transistors (c and d). The topography and surface potential scans were collected in two sequential scans at each contact because the length of the channel was larger than the scan window. The surface potential profiles have been offset along the y-axis for clarity.

broadening of the individual peaks. A new peak at $2\theta \sim 38.3°$ corresponding to the (111) plane of the gold overlayer is observed.[36] While we are not able to quantify the extent of crystallinity before and after gold evaporation due to attenuation of the X-ray intensity from the gold overlayer, these results unambiguously indicate that TES ADT remains largely crystalline and that the crystal structure of the thin film is preserved even after exposure to gold evaporation.

We also carried out direct imaging experiments with AFM in hopes of elucidating the origin of the reduced current in top- versus bottom-contact thin-film transistors. Specifically, we interrogated TES ADT after it had been crystallized by solvent−vapor annealing and crystalline TES ADT after it had been exposed to gold evaporation. To characterize the underlying TES ADT layer, the evaporated gold was peeled away with Scotch tape. As a control experiment, we also examined regions of crystalline TES ADT that were protected by a shadow mask during gold evaporation (corresponding to the channel regions in actual devices). The topographical images acquired during these experiments are presented in Figure 5. While TES ADT does not appear to be chemically or structurally different before and after gold evaporation, the topographical features obtained on the samples before and after evaporation are very distinct. Specifically, we observe a pitted morphology in TES ADT after it had been exposed to gold evaporation (Figures 5b and 5e). This pitted morphology is not observed in the pristine TES ADT film (Figures 5a and 5d) or in the regions protected by the shadow mask (Figures 5c and 5f). Separately, we also carried out imaging experiments on crystalline TES ADT films that were not exposed to gold evaporation but were subjected to the Scotch tape peel test. These films look like the pristine films and do not exhibit any pitting. The pitted morphology must therefore stem from local damage during direct gold evaporation. Given the absence of any chemical changes during gold evaporation, we attribute this damage to localized melting of TES ADT when it is exposed to the energetic gold flux during evaporation. This local melting in turn creates structural disorder at the electrode−channel interfaces, which subsequently hinders charge injection and extraction.

To examine aspects of charge injection into and charge extraction out of TES ADT in bottom- and top-contact thin-film transistors in more detail, we conducted scanning surface potential measurements (SSPM)[23−25] on these devices. The SSPM results for a bottom- and top-contact TES ADT thin-film transistor are shown in Figure 6. The topography images collected for both transistors clearly show the source and drain electrodes as well as the channel region of each transistor (Figures 6a and 6b). Figures 6c and 6d contain the surface potential profiles collected across the channels of the bottom- and top-contact devices, respectively. These figures show how the −2 V bias applied between the source and drain electrodes is distributed across the channel during device operation (gate bias is increased from 0 to −20 V in increments of −4 V). We observe sharp potential drops at the gold−TES ADT interface, followed by a gradual drop across the channel, and another sharp drop at the other gold−TES ADT interface. Further, the potential drops at the source and drain electrodes are significantly smaller in the bottom-contact transistor (Figure 6c) compared to that in the top-contact transistor (Figure 6d). Consistent with our AFM results, this comparison suggests that both charge injection and charge extraction are more efficient in the bottom-contact transistor compared to those in the top-contact transistor of comparable channel geometry and dimensions. During the surface potential measurements, we simultaneously collected the source−drain current. Ohm's law thus allows for extraction of the channel resistance and the contact resistances at the electrode−channel interfaces. The channel and contact resistances calculated for the bottom- and top-contact transistors are tabulated in Table 1. Since the TES ADT channel region is protected by a shadow mask during gold evaporation, we expect the channel resistance to be comparable in both transistors. Quantification of the channel resistances in both devices indicates that they are in fact similar ($\sim 1 \times 10^6\ \Omega$). We do, however, expect a significant

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Table 1. Channel and Contact Resistances Extracted from Surface Potential Measurements on Bottom- and Top-Contact TES ADT Thin-Film Transistors

transistor geometry	$R_{channel}$	R_{source}	R_{drain}
bottom contact	$9.6 \times 10^5\ \Omega$	$3.5 \times 10^5\ \Omega$	$2.4 \times 10^5\ \Omega$
top contact	$1.1 \times 10^6\ \Omega$	$6.6 \times 10^6\ \Omega$	$3.6 \times 10^6\ \Omega$

difference in the contact resistances at the electrode−channel interfaces based on the observed surface potential drops and the disparity in performance between bottom- and top-contact transistors. As shown in Table 1, the contact resistances at both the source and drain electrodes are at least an order of magnitude higher in the top-contact transistor compared to those in the bottom-contact transistor. While this result contradicts previous literature reports which show that bottom-contact transistors exhibit higher contact resistance than top-contact transistors,[31,37] it is consistent with our macroscopic current−voltage characterization and our AFM data, and it further implicates the consequences of local melting of TES ADT.

We have thus devised an alternative means of making electrical contact to TES ADT in the top-contact configuration. Specifically, we built top-contact TES ADT thin-film transistors by soft-contact lamination.[17−20] With this technique (Figure 7), TES ADT is spun and crystallized on silicon dioxide in the exact manner as discussed previously. Gold source and drain electrodes, fabricated on a poly(dimethylsiloxane) (PDMS) stamp, are nondestructively contacted against the crystalline TES ADT film. This process is reversible; the PDMS stamp containing gold source and drain electrodes can be removed from the substrate without damaging the organic semiconductor thin film so multiple PDMS stamps with source and drain electrodes of varying geometry and dimensions can be contacted against the same substrate. Typical current−voltage characteristics of a laminated top-contact thin-film transistor are shown in Figure 2d. This laminated device exhibits higher on currents and charge-carrier mobility (0.24 $cm^2/V\cdot s$) compared to those of the top-contact thin-film transistors with gold electrodes defined by direct evaporation (0.08 $cm^2/V\cdot s$; Figure 2c) and the bottom-contact transistor (0.2 $cm^2/V\cdot s$; Figure 2a) with equivalent channel dimensions. Of the 39 laminated devices tested, the average charge-carrier mobility was 0.19 ± 0.06 $cm^2/V\cdot s$.

(37) Necliudov, P. V.; Shur, M. S.; Gundlach, D. J.; Jackson, T. N. *Solid-State Electron.* **2002**, *47*, 259.

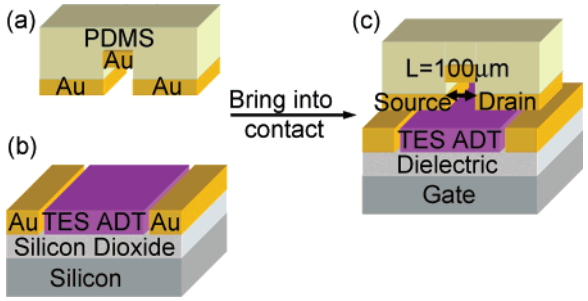

Figure 7. Soft-contact lamination scheme. (a) Titanium (2 nm) and gold (20 nm) are deposited onto a PDMS stamp with source and drain features. (b) TES ADT is spin-coated and annealed on a silicon substrate with 100 nm of thermally grown silicon dioxide. Gold contact pads (40 nm) are subsequently evaporated around the TES ADT film. (c) The PDMS stamp containing the source and drain electrodes is then contacted against the TES ADT film so the gold features on the PDMS stamp contact both the TES ADT film and gold contact pads. The recessed region of the stamp defines the channel of the thin-film transistor.

Conclusions

The materials properties of the organic semiconductor play a significant role in choosing the appropriate electrode fabrication method to achieve optimal device performance. In the case of TES ADT, this material forms weak crystals on crystallization, thereby rendering the material susceptible to thermal damage when exposed to direct gold evaporation. As a result of this local melting, defects are created at the electrode−channel interfaces, which can severely hamper charge injection and extraction in top-contact thin-film transistors. Macroscopically, top-contact devices exhibit reduced charge-carrier mobility compared to bottom-contact devices with equivalent dimensions. Reduced device performance can be avoided if top-contact thin-film transistors are fabricated by nontraditional patterning methods, such as soft-contact lamination, which nondestructively establish electrical contact to the organic semiconductor. These results imply that patterning methodologies for establishing electrical contact will have to satisfy the materials limitations of inherently fragile organic semiconductors.

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